Comparison of short-channel effects in monolayer MoS_2 based junctionless and inversion-mode field-effect transistors

Tarun Agarwal' , Bart Sorée, Iuliana Radu, Praveen Raghavan, Gianluca Fiori, Giuseppe Iannaccone, Aaron Thean, Marc Heyns, and Wim Dehaene

Citation: Appl. Phys. Lett. **108**, 023506 (2016); doi: 10.1063/1.4939933
View online: http://dx.doi.org/10.1063/1.4939933
View Table of Contents: http://aip.scitation.org/toc/apl/108/2
Published by the American Institute of Physics

Comparison of short-channel effects in monolayer MoS_2 based junctionless and inversion-mode field-effect transistors

Tarun Agarwal,[1,2,a)] Bart Sorée,[1,2,3] Iuliana Radu,[2] Praveen Raghavan,[2] Gianluca Fiori,[4] Giuseppe Iannaccone,[4] Aaron Thean,[2] Marc Heyns,[2] and Wim Dehaene[1]
[1]*Department of Electrical Engineering, Katholieke Universiteit Leuven, Heverlee 3001, Belgium*
[2]*Interuniversity Microelectronics Centre (IMEC), Heverlee 3001, Belgium*
[3]*Department of Physics, Universiteit Antwerpen, 2020 Wilrijk, Belgium*
[4]*Dipartimento di Ingegneria dell'Informazione, Universita' di Pisa, Via Caruso 16, 56122 Pisa, Italy*

(Received 5 August 2015; accepted 13 December 2015; published online 15 January 2016)

Conventional junctionless (JL) multi-gate (MuG) field-effect transistors (FETs) require extremely scaled channels to deliver high on-state current with low short-channel effect related leakage. In this letter, using ultra-thin 2D materials (e.g., monolayer MoS_2), we present comparison of short-channel effects in JL, and inversion-mode (IM) FETs. We show that JL FETs exhibit better sub-threshold slope (S.S.) and drain-induced-barrier-lowering (DIBL) in comparison to IM FETs due to reduced peak electric field at the junctions. But, threshold voltage (V_T) roll-off with channel length downscaling is found to be significantly higher in JL FETs than IM FETs, due to higher source/drain controlled charges (dE/dx) in the channel. Further, we show that although V_T roll-off in JL FETs improves by increasing the gate control, i.e., by scaling the oxide, or channel thickness, the sensitivity of threshold voltage on structural parameters is found out to be high.
 [http://dx.doi.org/10.1063/1.4939933]

Novel materials and device structures have been explored in order to continue scaling of MOSFET devices. Multi-gate (MuG) field-effect transistors (FETs), due to their excellent gate control, are being pursued for current, and upcoming technology nodes. Moreover, junctionless (JL) MuGFET has been proposed as a potential future device option showing better scalability, and fabrication simplicity in comparison to inversion-mode (IM) FETs. Due to its operation based on pinch-off of the channel by means of depletion, JL FETs require extremely scaled channels, or body in order to achieve better gate control, and low leakage.[1,2]

Recently, the emergence of a class of 2D semiconducting materials such as transition metal dichalcogenides (TMDs) have enabled the possibility of atomic thin channels in FETs for better gate control. For example, monolayer MoS_2 FET has been shown to have better scalability than an ultra-thin-body (UTB) Si FET due to monolayer thin body, and higher effective mass, resulting in reduced direct source-to-drain tunneling.[3] Moreover, a sub-threshold slope (S.S.) of 60 mV/dec has been demonstrated in monolayer WSe_2 FET.[4]

In this letter, we present a study discussing channel length scaling of monolayer MoS_2 based junctionless and inversion-mode FETs. Using atomistic two-band ballistic quantum transport simulations, we show that JL FETs promise better scalability than IM FETs considering short-channel effects (SCEs) such as S.S. and drain-induced-barrier-lowering (DIBL). But, surprisingly JL FETs show worse threshold voltage (V_T) control with channel length downscaling in comparison to IM FETs, resulting in higher V_T roll-off. We further discuss the underlying mechanism for such improvement in S.S. and DIBL, and reduction of threshold voltage with channel length downscaling. It is explained that although JL FETs manifest reduced electric field at the junctions in comparison to IM FETs, JL FETs also show higher gradient of lateral electric field in channel, i.e., higher source/drain controlled charges, and thus lower V_T with channel length downscaling. We further show that we require better gate control in JL FETs than IM FETs for lower V_T roll-off, which can be achieved by further scaling the oxide thickness or the channel thickness.

Monolayer MoS_2 based IM and JL FETs in double-gate configuration are schematically shown in Fig. 1. It is important to note here that we use abrupt source/drain junctions, and no gate overlap in IM FETs to compare both non-optimized IM and JL FETs with same structural parameters such as oxide thickness (t_{HfO_2}) and channel length (L_{CH}). Moreover, we use

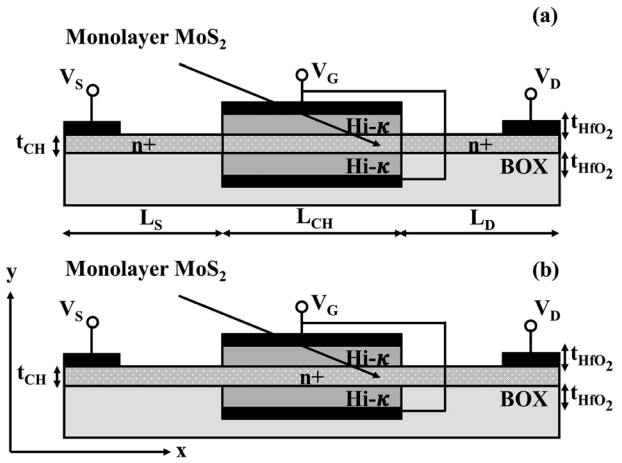

FIG. 1. Schematic of monolayer MoS_2 based (a) inversion-mode FET and (b) junctionless FET in double-gate configuration with $L_S = L_D = 15$ nm, n^+ doping of 1.5×10^{13} cm^{-2}, $t_{HfO_2} = 4.9$ nm with $\epsilon_{HfO_2} = 25$, $t_{CH} = 0.7$ nm, and $L_{CH} = 6$–30 nm.

a)Electronic mail: Tarun.AgarwalKumar@imec.be.

same doping concentration of 1.5×10^{13} cm^{-2} for n^+ doping in JL FETs, and source/drain regions for IM FETs using similar chemical doping techniques as demonstrated in Ref. 4, while the MoS_2 channel in IM FET is assumed to be intrinsically n^- doped from the environment, as reported in experimental works such as in Ref. 5. The electrical characteristics of both IM and JL FETs are simulated using two-band tight binding (TB) Hamiltonian with an open source quantum transport simulation framework based on self-consistent solution of Poisson and Schrödinger equation in non-equilibrium Green's function framework.[6] Further, the two-band Hamiltonian can be defined as a 2×2 Hamiltonian matrix, which is based on a unit cell of two-dissimilar atoms such M and X in MX_2 materials, and can be written as

$$H_{CH} = \begin{bmatrix} E_C & tf(k) \\ tf^*(k) & E_V \end{bmatrix}, \tag{1}$$

where E_C and E_V represent bottom of conduction band and the top of the valence band, which is related to bandgap (E_G) of the material as: $E_G = E_C - E_V$. While t represents in-plane hopping energy which is fitted for a specific effective mass (m*), and $f(k)$ function, due to nearest neighbors, can be written as

$$f(k) = e^{\left(ik_y a/\sqrt{3}\right)} + 2e^{\left(-ik_y a/2\sqrt{3}\right)} \cos\left(\frac{k_x a}{2}\right). \tag{2}$$

Here, k_x and k_y are wave vectors in x and y directions of our device, while a represents distance between M and X atoms. Further, using secular equation, we obtain dispersion relation for two-band model given as

$$E^{\pm}(k) = \frac{(E_C + E_V) \pm \sqrt{(E_C - E_V)^2 + 4t^2|f(k)|^2}}{2}, \tag{3}$$

which provides a good approximation for lowest conduction band, and highest valance band of monolayer MX_2 materials for the considered bias ranges. For monolayer MX_2 materials, the two-band Hamiltonian parameters are calculated using the effective mass of conduction (n-FET) or valence band (p-FET), and bandgap of the material.[7] Further, we extend the model for bilayer MX_2 materials using an inter-layer hopping parameter in the Hamiltonian, accounting for inter-layer coupling between the two layers.[8] Here, monolayer MoS_2 channel is modeled with an electron effective mass of 0.45 m_0, and bandgap energy of 1.8 eV, while the bilayer MoS_2 channel is modeled with an electron effective mass of 0.62 m_0 and a bandgap of 1.3 eV.

With different gate work functions for IM ($\phi_M = 4.6$ eV) and JL FETs ($\phi_M = 5.4$ eV), the transfer characteristics of both FETs are shown in Fig. 2 with channel length scaling. We can observe that JLFET with monolayer MoS_2 shows better electrostatic integrity with channel length (L_{CH}) downscaling. To have a closer look at SCE parameters, we plot S.S., DIBL, and V_T roll-off extracted from transfer characteristics of IM and JL FETs, as shown in Fig. 3. Here, V_T is extracted from transfer characteristics of both FETs using constant current method at a given normalized drain current $(I_D/W) = I_{ref}/L_{CH}$, where W is the width of the channel, and I_{ref} is chosen to be 250 nA. It can be seen from Fig. 3(a) that JL FET shows lower S.S. and DIBL with channel length downscaling in comparison to conventional inversion-mode FET, as reported in literature for multi-gate FETs.[9] But, surprisingly JL FETs show worse threshold voltage (V_T) control with channel length scaling in comparison to IM FETs, as shown in Fig. 3(b).

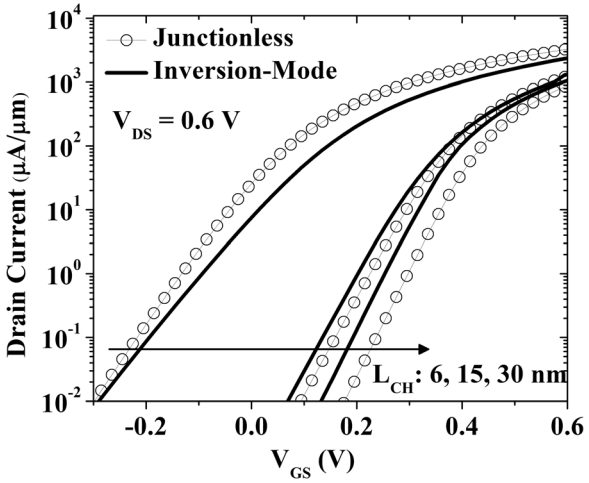

FIG. 2. Transfer characteristics of monolayer MoS_2 based double-gate inversion-mode, and junctionless FETs for channel lengths (L_{CH}) of 6, 15, and 30 nm.

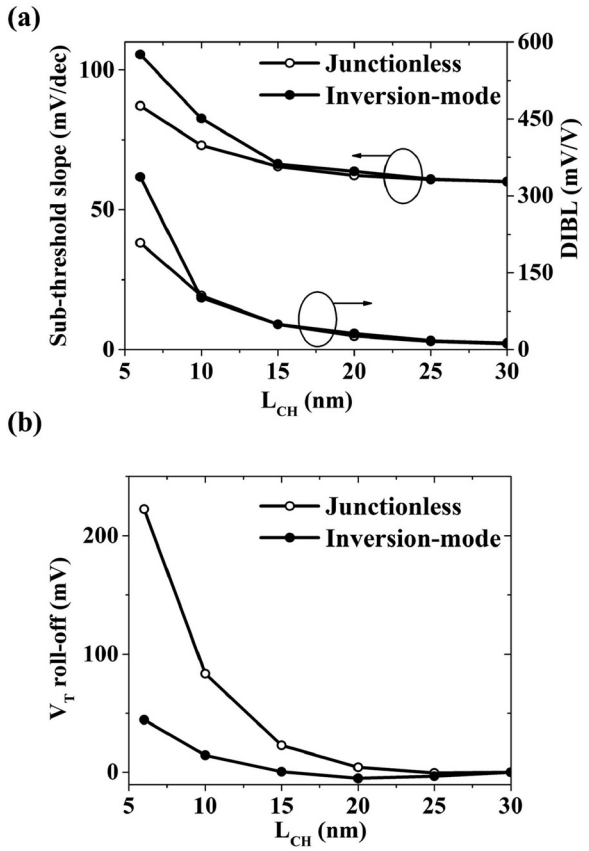

FIG. 3. Short channel effects in monolayer MoS_2 based IM and JL FETs. (a) Sub-threshold slope, and DIBL with channel length scaling, and (b) V_T roll-off with channel length scaling. Here, V_T roll-off signifies threshold voltage (V_T) difference at smaller channel lengths with respect to $L_{CH} = 30$ nm, i.e., V_T roll-off$(L_{CH}) = V_T(L_{CH} = 30\,\text{nm}) - V_T(L_{CH})$.

To understand the underlying mechanism for such improvement in S.S. and DIBL, we plot the off-state conduction band energy minima (E_C) along the channel, showing the source-to-channel barrier in off-state ($V_T - 1/3*V_{DD}$) which effectively determines the off-state current. Fig. 4(a) shows the off-state E_C(x) along the channel at the middle of the width of monolayer MoS_2 channel. It can be observed from Fig. 4(a) that both height and width of source/channel barrier are larger for JL FETs in comparison to IM FETs. The larger width of the barrier prevents source-to-drain direct tunneling components, resulting in overall lesser leakage current. Further, as shown in Fig. 4(b), the absolute value of lateral electric field at source/channel, and channel/drain junctions are significantly lower in JL FETs in comparison to IM FETs, resulting in larger depletion lengths inside the drain extension, and thus lowering the effect of drain bias on source/channel barrier in JL FETs. Deep depletion inside source/drain extensions has been reported to result in improvement in S.S. and DIBL in JL FETs in comparison to IM FETs, which effectively results in larger width of the barrier and lower lateral electric fields at the junctions in JL FETs.[10,11]

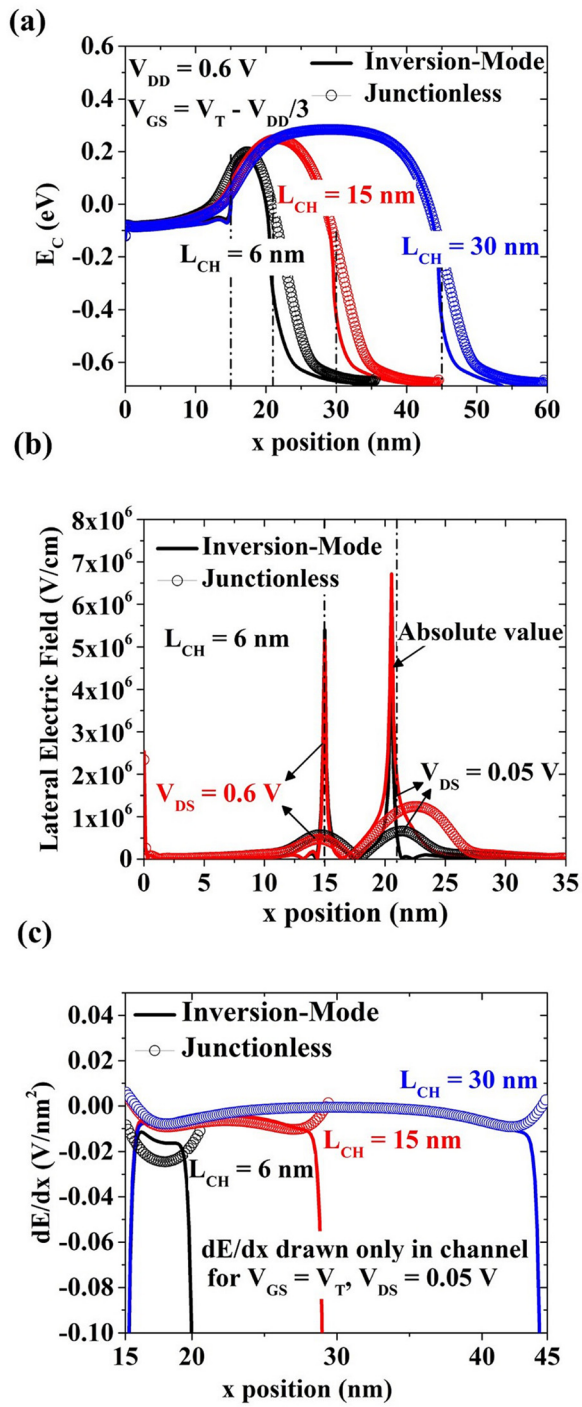

FIG. 4. Underlying mechanism for short channel effects in monolayer MoS_2 based IM and JL FETs. (a) Conduction band energy minima (E_C) along the channel direction for different channel lengths, and (b) absolute value of lateral electric field for low, and high drain-to-source voltage (V_{DS}) along the channel direction for $L_{CH} = 6$ nm. (c) Gradient of lateral electric field representing source/drain controlled charges in the channel for different channel lengths.

But, surprisingly JL FET exhibits larger V_T roll-off in comparison to IM FET due to higher source/drain controlled charges inside channel at downscaled channel lengths. To understand it quantitatively, we can write charge density inside monolayer MoS_2 channel (n_{2D}) as

$$n_{2D} = n_G + n_{SD}. \tag{4}$$

Here, n_G for a symmetrical double-gate FET is obtained as

$$n_G = 2C_G(V_{GS} - V_{FB} - \phi(x)). \tag{5}$$

where C_G, V_{FB}, and $\phi(x)$ represent the effective gate capacitance including quantum capacitance expressed in F/cm^2, flat-band voltage, and surface potential inside channel, respectively. While n_{SD} can be written as

$$n_{SD} = \frac{\epsilon_{CH} t_{CH}}{q}\left(\frac{dE}{dx}\right), \tag{6}$$

where ϵ_{CH} and q represent dielectric constant of monolayer MoS_2 channel and electron charge, respectively. Eq. (6) establishes a direct relationship of source/drain controlled charges on gradient of lateral electric field. As shown in Fig. 4(c), dE/dx inside the channel increases significantly in JL FETs with channel length scaling in comparison to IM FETs, resulting in larger V_T roll-off in JL FETs.

From the discussion above, we show that S.S., DIBL, and V_T roll-off for JL FETs need to be analyzed differently from IM FETs, as JL FETs operate on a principle of depleting the channel rather than inverting it. Therefore, for S.S. and DIBL, we look at the electrostatic potential/electric field profiles at the junctions and outside the channel, as the improvement in S.S. and DIBL for JL FETs arises due to deep depletion in source/drain regions, thus resulting in reduced electric field at the junctions, and direct source to drain tunneling. While for threshold voltage (V_T) roll-off, we calculate the charges present inside the channel, which consists of gate and source/drain controlled charges.

Further, we can write source/drain charges controlled component of threshold voltage (V_T) as

$$V_{TL} = \lambda_{2D}^2 \frac{dE}{dx}, \tag{7}$$

where λ_{2D} is the characteristic (scaling) length of symmetrical double-gate 2D material based FET, which can be written as[12]

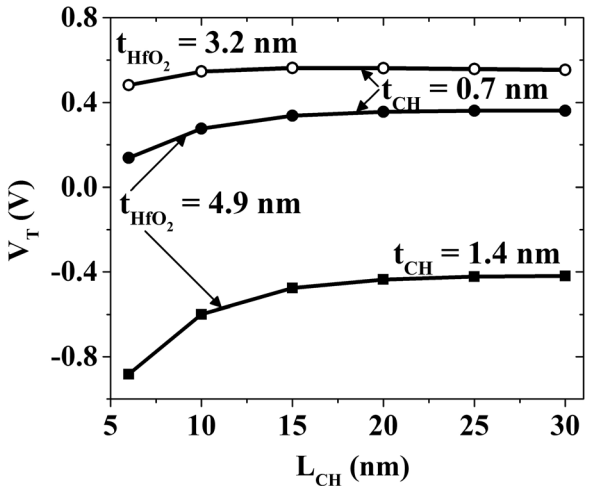

FIG. 5. Impact of scaling the oxide thickness and channel thickness on threshold voltage in JL FETs.

$$\lambda_{2D} = \frac{t_{HfO_2} + t_{CH} + t_{HfO_2}}{\pi}. \tag{8}$$

Thus, improving the gate control (i.e., lowering λ_{2D}) promises to improve V_T control in JL FETs with channel length downscaling. Fig. 5 shows that although there is an improvement in V_T roll-off by scaling the oxide or channel thickness, we observe that V_T of JL FETs is highly sensitive to structural parameters such as oxide thickness and channel thickness. Moreover, it is important to note here that from electrostatic perspective JL FETs may perform inferior to IM FETs in case of thicker channels materials, due to increased equivalent-oxide-thickness in JL FETs.

In this letter, we present comparison of short-channel effects of monolayer MoS_2 based JL, and IM FETs. We show that although JL FET shows better electrostatic integrity from S.S. and DIBL point of view, it shows worse threshold voltage (V_T) control with channel length downscaling in comparison to IM FET. Further, due to larger dE/dx in channel, an increased gate control by scaling the oxide thickness does not result in a significant improvement in V_T roll-off of JL FETs. Poor threshold-voltage control in JL FETs may give rise to problems for circuit designers while using JL FETs in digital logic circuits, arising the need of adaptive biasing.

[1]B. Sorée, W. Magnus, and G. Pourtois, J. Comput. Electron. **7**(3), 380 (2008).
[2]J.-P. Colinge, C.-W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, P. Razavi, B. O'Neill, A. Blake, M. White, A.-M. Kelleher, B. McCarthy, and R. Murphy, Nat. Nanotechnol. **5**(3), 225 (2010).
[3]L. Liu, Y. Lu, and J. Guo, IEEE Trans. Electron Devices **60**(12), 4133 (2013).
[4]H. Fang, S. Chuang, T. C. Chang, K. Takei, T. Takahashi, and A. Javey, Nano Lett. **12**(7), 3788 (2012).
[5]B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti, and A. Kis, Nat. Nanotechnol. **6**(3), 147 (2011).
[6]See http://vides.nanotcad.com/vides for NanoTCAD ViDES.
[7]See http://vides.nanotcad.com/vides/documentation/tutorials/tutorial-17-transition-metal-dichalcogenides-based-fet for NanoTCAD ViDES.
[8]G. Fiori and G. Iannaccone, "Performance analysis of graphene bilayer transistors through tight-binding simulations," in *13th International Workshop on Computational Electronics (IWCE)* (2009), pp. 1–4.
[9]C.-W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, and J.-P. Colinge, Appl. Phys. Lett. **94**, 053511 (2009).
[10]J.-P. Colinge, C.-W. Lee, I. Ferain, N. D. Akhavan, R. Yan, P. Razavi, R. Yu, A. N. Nazarov, and R. T. Doria, Appl. Phys. Lett. **96**, 073510 (2010).
[11]Y. Song and X. Li, Appl. Phys. Lett. **105**, 223506 (2014).
[12]H. Ilatikhameneh, G. Klimeck, J. Appenzeller, and R. Rahman, IEEE Electron Device Lett. **36**(7), 726 (2015).